Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **1CLK**
2. **1CLR**
3. **1K**
4. **VCC**
5. **2CLK**
6. **2CLR**
7. **2J**
8. **N. 2Q**
9. **2Q**
10. **2K**
11. **GND**
12. **1Q**
13. **N. 1Q**
14. **1J**

**.065”**

**2 1 14**

**3**

**4**

**5**

**6**

**7 8**

**13**

**12**

**11**

**10**

**9**

**.065”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: GND**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .065” X .065” DATE: 3/24/21**

**MFG: SIGNETICS THICKNESS .015” P/N: 54LS73**

**DG 10.1.2**

#### Rev B, 7/1